The Comparison of Analogue and Digital One-Cycle Control Feedback Methods around the Output Stage in a Digital Audio Power Amplifier

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Abstract – A digital amplifier has benefits such as reduced power consumption and a smaller, lightweight form factor. However, for the Hi-Fidelity audio market, the quality of this amplifier configuration is typically lacking as many sources of error have been identified around the output stage in a switching amplifier. The One-Cycle Control scheme is a solution which has the ability to eliminate many of these errors in a single cycle. Current implementations have been of an analogue form, but due to the nature of a digital amplifier, it is reasonable to include this feedback control in the digital domain. Therefore, a digital form of One-Cycle Control is being developed, and is being compared to the analogue version. If successful, this digital implementation will be incorporated into commercial high-power, high-fidelity audio amplifiers by Perreaux Industries Ltd.

1. INTRODUCTION

Audio power amplifiers targeted at the Hi-Fidelity market have typically been of a Class-A or Class-AB topology as Hi-Fidelity audio quality is easily and readily obtained with these configurations. However, these amplifiers are usually bulky and very inefficient with a typical amplifier reaching only 40-70% efficiency [1]. With the market today demanding a higher power output with a focus on energy and resource conservation, a smaller and more efficient amplifier is desirable.

The switching (or digital) amplifier has a significantly improved efficiency compared to the Class-A and AB techniques. However, until recently it has not been feasible to use this type of amplifier in a Hi-Fidelity audio environment. With the advancement of digital processing techniques, it has been possible to improve the Pulse Width Modulated (PWM) signal generation process, and recent research around the output stage has seen an increase in the number of switching-type amplifiers available to consumers. However, many of the available amplifiers are of a Class-D configuration or similar, and are not compatible with a digital audio format. Also, the digital amplifiers that are available still leave room for improvement.

It is proposed that if a digital amplifier can be developed to perform to an equal or better standard than that of the current linear amplifiers available (as far as the human ear is concerned) then this new digital amplifier technology would have significant market potential. In quantitative terms, this typically means an amplifier with a Signal-to-Noise Ratio (SNR) of better than 96 dB (CD Quality), and a Total Harmonic Distortion (THD) of less than 0.01 %.

2. BACKGROUND

The common Class-A and Class-AB classes of amplifier are an analogue form of amplification where the devices in the output amplification stage spend the majority of time operating in their linear region. This means that these devices are dissipating power for the majority of the audio cycle and thus the amplifier is rather inefficient and bulky due to the large heat sinks required.

A common solution is a lighter, cheaper and more efficient form of amplifier commonly called a switching amplifier. A switching amplifier is typically based around the concept of a PWM signal where the width of each pulse is proportional to the amplitude of the analogue control signal being amplified. In such an amplifier, this PWM signal is what is amplified, thus the devices in the output stage are ideally either on or off, and never operate in the linear region at any time. The resulting amplified PWM signal is then filtered with a low-pass filter to remove the switching component, and the resulting audio signal is delivered to the loudspeaker. Such an amplifier can reach efficiencies greater than 90 % [2,3,4].

The switching amplifier is commonly implemented as a Class-D type. A Class-D amplifier takes an analogue audio input signal and from this generates the PWM signal to be amplified. To achieve this, a reference triangle-wave signal is generated, and this is compared with the audio signal. These signals are shown in Figure 1, which shows that when the audio signal is greater than the triangle-wave, the PWM output is high (1), and when the audio signal is less than the triangle-wave, the PWM output is low (0).

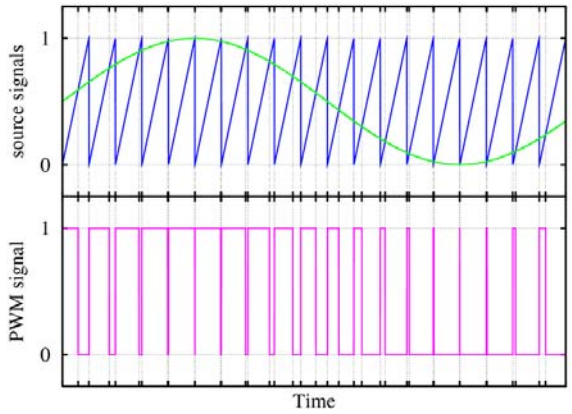

Figure 1: Source, reference triangle wave and resulting PWM signals.

However, in a digital amplifier the input is taken from a digital representation of the audio, such as Pulse Code Modulation (PCM) encoded audio or Sony/Philips Digital Interconnect Format (SPDIF), and the PWM signal is generated in the digital domain. Digital amplifiers have become an increasingly active research topic in recent years, especially as its application to consumer audio has become apparent [5,6].

In this case, the PWM signal cannot be derived with an analogue circuit using the method above. A simplified block diagram for a digital amplifier is shown in Figure 2, and the focus of this paper is on feedback methods around the output stage.

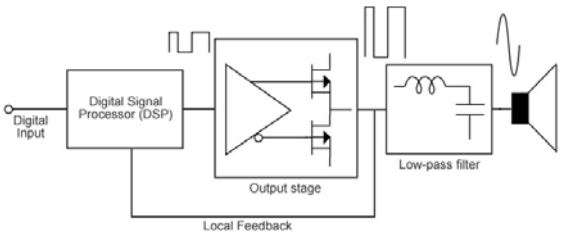

Figure 2: Digital Amplifier Block Diagram

3. SOURCES OF ERROR

There are many sources of error in the output stage leading to an amplified PWM signal that is far from ideal. Sources of error, as shown in Figure 3, include power supply ripple, voltage drops from the switching devices (typically MOSFETs, and sometimes flyback diodes), overshoot and undershoot, rise and fall times and turn on and turn off delays. Each of these unwanted artifacts is a source of THD in the resulting output audio signal.

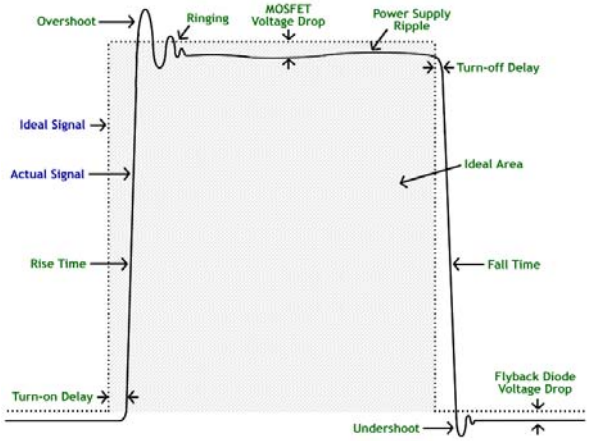

Figure 3: Sources of Error in the Switching Converter

To overcome these sources of error, a feedback control is required to provide corrective measures. This can be achieved by adjusting the duty-cycle of the PWM signal accordingly. Although several feedback methods have been discussed previously [7,8,9], the focus of this paper is on One-Cycle Control [10,11] as it can correct for errors in a single PWM cycle period allowing for a faster correction and therefore resulting in a more accurate PWM signal.

4. ONE-CYCLE CONTROL

The feedback around the output stage is called One-Cycle Control [10,11] where the integration of each period of the PWM signal is forced to a value that is equal to, or proportional to, the control reference.

Previously, One-Cycle Control has been implemented in the analogue domain as shown in Figure 4. The circuit includes an integrator (*INT*) to integrate the area under the PWM output signal over time, and a comparator (*CMP*) to compare the integrator output to a control reference voltage. As shown in Figure 5, when the integrator output *Vint* reaches the reference value -*Vref*, the PWM driving signal changes state and the integrator is reset. These signals are depicted in Figure 5 and show how the reference signal is negative for a PWM duty cycle of greater than 50 %, as the output PWM signal is the inverse of the driving PWM signal $\bar{Q}$.

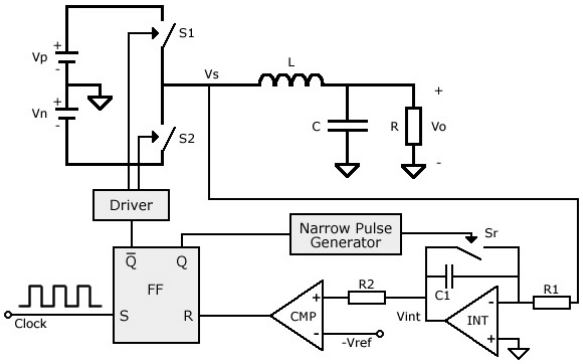

Figure 4: One-Cycle Control

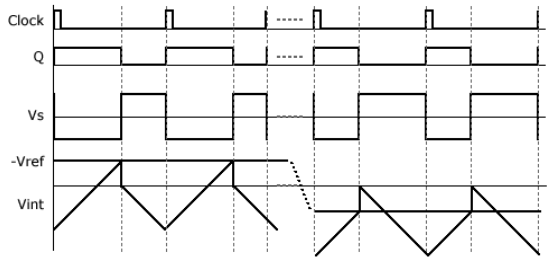

Figure 5: One-Cycle Control Waveforms

The act of resetting of the integrator circuit every cycle is performed by discharging capacitor *C1* via switch *Sr*. It has been found that an error is introduced due to the finite time taken to discharge the capacitor [12]. This leads to a reduction in the area under the output PWM signal, and therefore results in an output that is non-linear. Another problem with an analogue circuit is that the low voltage signals in the analogue One-Cycle Control circuitry are prone to noise coupled from the relatively high voltage output stage. Furthermore, due to the nature of a digital amplifier, the control reference signal resides in the digital domain, and thus a conversion to an analogue reference signal, via a Digital-to-Analogue Converter (DAC) is required for the One-Cycle Control circuitry.

5. THE DIGITAL IMPLEMENTATION

A digital implementation of the One-Cycle control method is proposed in an attempt to eliminate the problems associated with the analogue version and is shown in
Figure 6. As the control reference in a digital amplifier is already in the digital domain, it makes sense to implement the One-Cycle Control algorithm in the digital domain also. As shown, the switched output signal Vs is divided down to a suitable voltage via a resistor divider consisting of R1 and R2, and fed into the Analogue-to-Digital Converter (ADC). The digital values are then read from the ADC by a logic circuit in the Programmable Logic Device (PLD) which performs a digital summation and comparison, and generates the signals for the Driver.

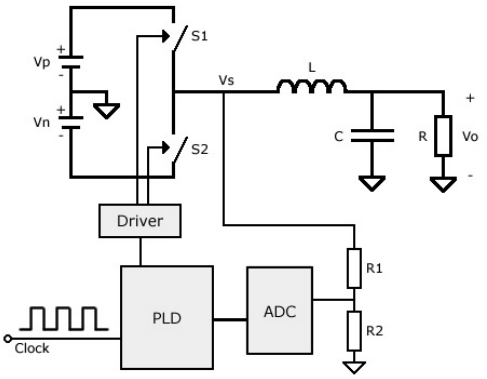

Figure 6: Digital form of One-Cycle Control

The primary benefit of the digital implementation is the elimination of the requirement to reset an analogue integrator. The digital equivalent of this function is simply to clear or reset a digital counter back to zero or a predefined value. This can be achieved by a PLD logic circuit in a single clock cycle, and with a conservative clock frequency of 150 MHz, this equates to a time of less than 7 ns.

Another benefit of the digital implementation is that any noise generated from the higher voltages and large transient currents involved in the output stage will not affect the operation of the logic circuit and thus the control results are essentially immune. There is also a potential reduction in component count as much of the control can be performed inside a single PLD chip. Alternatively, this function can be performed within a digital processor that performs other signal processing functions, which is already present in many digital amplifier systems.

A further benefit of a digitally implemented One-Cycle Control is the ability to subtract the reference control value from the digital integrator rather than resetting the sum to zero. This means that any time domain errors associated with the sampling of the PWM signal can be accounted for, and corrected in the subsequent cycle. For example, if the integrator had a sum of 850, and a value of 100 was read from the ADC, while the target value was 900, then resetting the integrator to zero will cause an error of 50. However, if the target value was subtracted from the sum, the counter will begin the following cycle with a value of 50 (850 + 100 – 900), and the average of the two cycles will be correct. Not only is this almost impossible to achieve with an analogue implementation, but information is also lost during the time taken to reset the integrator.

However, the digital implementation of the One-Cycle Control method also has two disadvantages. Firstly, as the PWM output signal must be converted to a digital form via an Analogue-to-Digital Converter (ADC), a quantization error is introduced. Secondly, the limited clock frequencies of a digital circuit also introduce an error as the PWM output signal can only be sampled a finite number of times per second, and thus the potential

to lose error information present in the PWM output signal is introduced.

Work is currently underway to examine whether the benefits of a digital form of One-Cycle Control will outweigh the disadvantages. If it does, then this will lead to an overall reduction in the error component of the output PWM signal, and an improvement in the THD and SNR of the resulting output audio signal that is delivered to the loudspeaker is achieved.

6. PROGRESS

So far several prototype versions have been developed. The latest revision is two separate 4-layer circuit boards for a comparison between both the analogue and digital versions which are shown in Figure 7 and Figure 8. Both circuits include a Xilinx XC2C256 complex programmable logic device (CPLD) running at 150 MHz, and development and testing is being performed with an output PWM frequency of between 250 kHz and 800 kHz.

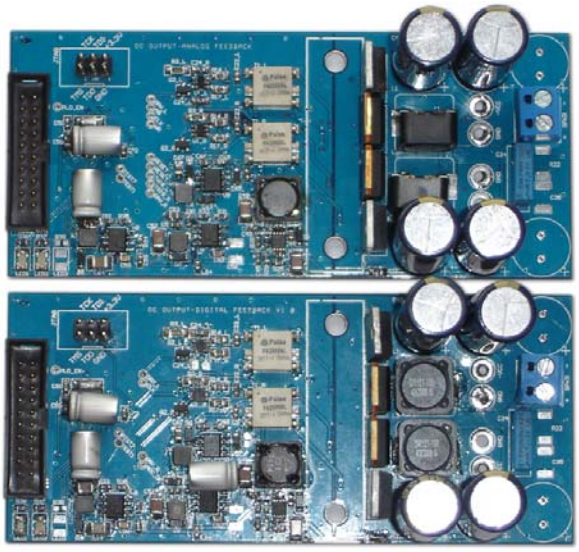

Figure 7: Prototype Analogue (Top) and Digital Digital (Bottom) One-Cycle Control Boards - Top View

The analogue prototype has a standard One-Cycle Control feedback implementation, where a digital reference signal is converted to an analogue reference voltage using a 16-bit ADC. A high speed op-amp with a sufficient slew rate has been chosen for the integrator function. Also, a small value for the capacitor (1 nF) has been chosen, combined with a low impedance analogue switch, to minimize the time to reset the integrator.

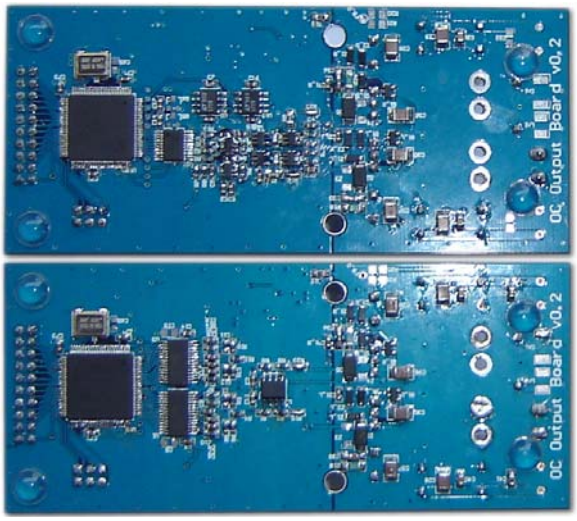

Figure 8: Prototype Analogue (Top) and Digital (Bottom) One Cycle Control Boards - Bottom View

The digital implementation uses a high frequency 10-bit ADC to convert the output PWM signal to a digital value at a rate of 75 million samples per second (MSPS). These values are fed into a digital integration counter and comparator circuit in the CPLD which generates the resulting PWM signal to be amplified. A tradeoff exists between the sampling frequency and resolution of the ADC. Of course, to get the most accurate feedback control, the PWM signal should be sampled at the highest possible frequency with the highest possible resolution (number of bits). However, the current technology available is somewhat limiting, and it is difficult to obtain a reasonably priced ADC that can operate above 100 MHz, with a resolution of 16 bits. Those that were able to be sourced cost over NZ$150 ea.

The two feedback circuits are operational and the investigation into comparison of the two amplifiers is currently ongoing. One issue that has arisen is an instability that occurs when the negative power supply rail is greater than the positive, which has been identified and discussed in [12]. The result is a sub-harmonic oscillation at half the switching frequency as shown by the pink trace in Figure 9. As the solution for the analogue implementation is to add a common offset to *Vs* and *-Vref*, an equivalent solution should exist for the digital implementation that can be included in the CPLD. However, the issue can be avoided for the purpose of comparative testing and is therefore not a concern.

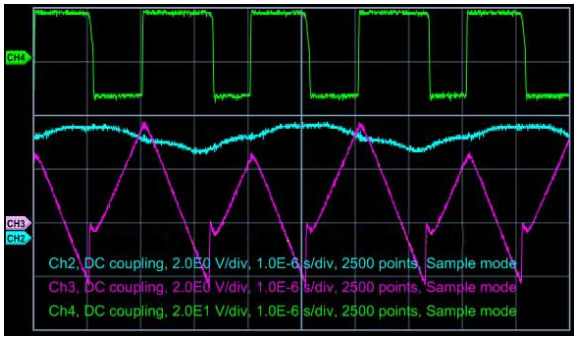

Figure 9: Sub-harmonic Oscillation in Analogue Feedback

Once some definitive comparative results have been obtained from the two prototypes, the effect of constraints such as the resolution and sampling frequency of the ADC, the clock frequency of the CPLD and the time taken to reset the integrator, will be clearer. At that stage, the feasibility of a digital implementation of One-Cycle Control will be determined, and its place in a commercial digital audio amplifier will be known.

7. REFERENCES

[1] Elliot, Rod. (1999). "Power Amplifier Efficiency Explained." from http://sound.westhost.com/efficiency.htm.

[2] Simon C. Li, Vincent Chia-Chang Lin. "A High Efficiency 0.5W BLT Class-D Audio Amplifier with RWDM Technique", Asia and South Pacific Design Automation Conference.,27-30 Jan 2004, pp. 307-309.

[3] Soo-Hyoung Lee, Jae-Young Shin, Ho-Young Lee, Ho-Jin Park, Kristian L. Lund, Karsten Nielsen and Jae-Whui Kim. "A 2W, 92% efficiency and 0.01% THD+N class-D audio power amplifier for mobile applications, based on the novel SCOM architecture", Custom Integrated Circuits Conference,3-6 Oct 2004, pp. 291-294

[4] Soo-Chang Choi, Jun-Woo Lee, Woo-Kang Jin, Jae-Hwan So and Suki Kim. "A Design of a 10W Single-Chip Class D Audio Amplifier with Very High Efficiency using CMOS Technology", IEEE Transactions on Consumer Electronics, **Vol. 45,** No. 3, Aug 1999, pp. 465-473.

[5] Sandler, Mark. "Digital Amplification for Consumer Audio", International Conference on Consumer Electronics (ICCE),June 2000, pp. 402-403.

[6] H D Farrar, R E Hiorns. "Development of a Commercial Digital Amplifier", Audio DSP - Circuits and Systems, **219,** Nov 1993, pp. 3/1-3/5.

[7] Pallab Midya, Bill Roeckner and Steve BergStedt. "Digital Correction of PWM Switching Amplifiers", IEEE Power Electronics Letters, **Vol. 2,** No. 2, June 2004, pp. 68-72.

[8] Jwu-Sheng Hu, Keng-Yuan Chen. "Implementation of a Full Digital Amplifier Using Feedback Quantization", American Control Conference,June 2006, pp. 2759-2764.

[9] Nielsen, Karsten. "PEDEC - A Novel Pulse Referenced Control Method for High Quality Digital PWM Switching Power Amplification", Power Electronics Specialists Conference, **Vol. 1,** May 1998, pp. 200-207.

[10] Zheren Lai, Keyue M. Smedley. "One Cycle Control of Bipolar Switching Power Amplifiers", US5617306, 1 April 1997, pp. 12.

[11] K. Smedley, S. Cuk. "One Cycle Control of Switching Converters", IEEE Transactions on Power Electronics, **Vol. 10,** No. 6, November 1995, pp. 625-633.

[12] Zheren Lai, Keyue M. Smedley. "A New Extension of One Cycle Control and Its Application to Switching Power Amplifiers", IEEE Transactions on Power Electronics, **Vol. 11,** No. 1, January 1996, pp. 99-105.